

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A multi clock deciding system comprising:
 - a master clock deciding apparatus (master) configured to output a system clock signal; [[and]]
 - a plurality of slave clock deciding apparatus ~~(slave)~~ apparatuses (slaves), each configured to generate a plurality of delay clock signals by delaying a reference clock signal, and to output a clock signal selected from the plurality of delay clock signals having a minimum phase difference from the system clock, ~~wherein the output of the master is inputted into the slave; and~~
 - a multi clock selecting unit configured to receive the clock signals output from the master and slaves and to supply the system clock signal to the master and slaves.
2. (Canceled)

3. (Currently Amended) The system of claim [[2]] 1, wherein the multi clock selecting unit outputs one of the slave clock outputs if there is an error on the clock signal of the master.

4. (Currently Amended) The system of claim [[2]] 1, wherein each clock deciding apparatus comprises:

 a phase locked loop (PLL) circuit configured to receive the reference clock signal and to output a P-clock signal;

 a signal delay unit configured to delay [[a]] the P-clock signal outputted from the PLL circuit to generate [[a]] the plurality of delay clock signals;

 a multiplexer configured to select and to output one of the delay clock signals;

 a phase comparing unit configured to detect an R-clock signal having the smallest phase difference from the system clock signal among the delay clock signals;

 an error detecting unit configured to detect an error on the reference clock signal and the system clock signal;

 a control unit configured to output a select control signal by referring to the result of the error detecting unit and an outer control signal; and

 a clock selecting unit configured to control the multiplexer by referring to the output of the phase comparing unit according to the select control signal.

5. (Original) The system of claim 4, wherein the clock selecting unit controls the multiplexer so as to output the P-clock signal when the control signal decides that the clock deciding apparatus is the master, and controls the multiplexer so as to output the R-clock signal if the control signal decides that the clock deciding apparatus is the slave.

6. (Original) The system of claim 4, wherein the clock deciding apparatus outputs the P-clock signal when an error is detected on the system clock signal.

7. (Original) The system of claim 4, wherein the signal delay unit comprises a plurality of signal delay elements.

8. (Original) The system of claim 4, wherein the delay clock signals have different delayed time from those of each other.

9. (Original) The system of claim 4, wherein the phase comparing unit detects the R-clock signal by comparing rising edge of the system clock signal to rising edge points of the respective delay clock signals.

10. (Currently Amended) The system of claim 4, wherein [[the]] each clock deciding apparatus generates the clock signal having a phase difference as much as an offset value with the system clock signal referring to the offset value.

11. (Original) The system of claim 10, wherein the offset value is variable.

12. (Currently Amended) The system of claim 1, wherein the slave is configured to:

convert the frequency of the reference clock into the frequency used in the system;

generate [[a]] the plurality of delay clock signals by delaying the converted reference clock signal (P-clock signal) for a predetermined time;

compare a phase of the system clock signal to phases of the respective delay clock signals; and

select and output one the delay clock signals having the smallest minimum phase difference from the system clock signal by referring to the phase comparison result.

13. (Original) The system of claim 12, wherein comparing phases compares the rising edges of the system clock signal and of the respective delay clock signals.

14. (Original) The system of claim 12, wherein the slave is further configured to detect an error on the reference clock signal and/or the system clock signal.

15. (Original) The system of claim 14, wherein the slave outputs the P-clock signal when the error is detected on the system clock signal.

16. (Currently Amended) ~~The system of claim 1, wherein A multi clock deciding system comprising:~~

a master clock deciding apparatus (master) configured to output a system clock signal; and

a slave clock deciding apparatus (slave) configured to generate a plurality of clock signals by delaying a reference clock signal, and to output a clock signal selected from the plurality of clock signals having a minimum phase difference from the system clock, wherein the output of the master is directly inputted into the slave and the output of the slave is directly inputted into the master,

17. (Currently Amended) A multi clock selecting method comprising:
generating a first output clock signal; [[and]]
generating a second output clock signal by[[::]] generating a plurality of delay clock signals by delaying a reference clock signal, and selecting one of the delay clock signals having a

minimum phase difference from the first clock signal as the second output clock signal;
receiving the output clock signals in a selecting unit; and
supplying a system clock signal from the selecting unit to respective clock devices
that generate the first and second output clock signals,
wherein the selecting unit outputs the second output clock signal as the system
clock signal if there is an error in the first output clock signal.

18-19. (Canceled)

20. (Currently Amended) The method of claim [[18]] 17, wherein ~~the~~each ~~an~~ output clock signal of each clock device is generated by:
generating a P-clock signal by inputting the reference clock signal into a phase locked loop (PLL) circuit;
delaying the P-clock signal to generate the plurality of delay clock signals;
detecting an R-clock signal having the ~~smallest~~ minimum phase difference from the system clock signal among the delay clock signals;
outputting a select control signal based on detecting an error on the reference clock signal and/or the system clock signal and an outer control signal; and
selecting the output clock signal according to the select control signal.

21. (Original) The method of claim 20, wherein selecting the output clock signal comprises:

outputting the P-clock signal if the control signal indicates that the clock device is a master; and

outputting the R-clock signal if the control signal indicates that the clock device is a slave.

22. (Original) The method of claim 20, further comprising:

outputting the P-clock signal when an error is detected on the system clock signal.

23. (Original) The method of claim 20, wherein the plurality of delay clock signals is generated by a plurality of signal delay elements.

24. (Currently Amended) The method of claim 20, wherein the plurality of delay clock signals each have different delay times.

25. (Original) The method of claim 20, wherein the R-clock signal is detected by comparing a rising edge of the system clock signal to rising edges of the delay clock signals.

26. (Currently Amended) The method of claim 17, wherein generating the second output clock signal further comprises:

converting a frequency of the reference clock into a system operating frequency;
generating the plurality of delay clock signals by delaying the converted reference clock signal (P-clock signal);
comparing a phase of the first clock signal to phases of the delay clock signals; and
selecting and outputting one of the delay clock signals having the ~~smallest~~
minimum phase difference from the first clock signal by referring to the phase comparison result.

27. (Currently Amended) The method of claim 26, wherein comparing the phases comprises:

comparing the rising edge of the first clock signal to rising edges of the delay clock signals.

28. (Original) The method of claim 26, further comprising:

detecting an error on the reference clock signal and/or the first clock signal.

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29. (Original) The method of claim 28, further comprising
outputting the P-clock signal when the error is detected on the first clock
signal.